Pseudomorphic HEMT Manufacturing Technology for Multifunctional Ka-Band MMIC Applications

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***Abstract*—We have demonstrated very good performance, high yield Ka-band multifunctional MMIC results using our recently developed 0.25-μm gate length pseudomorphic HEMT (PHEMT) manufacturing technology. Four types of MMIC transceiver components—low noise amplifiers, power amplifiers, mixers, and voltage controlled oscillators—were processed on the same PHEMT wafer, and all were fabricated using a common gate recess process. High performance and high producibility for all four MMIC components was achieved through the optimization of the device epitaxial structure, a process with wide margins for critical process steps and circuit designs that allow for anticipated process variations, resulting in significant performance margins. We obtained excellent results for the Ka-band power amplifier: greater than 26 dBm output power at center frequency with 4.0% standard deviation over the 3-in. wafer, 2-GHz bandwidth, greater than 20 percent power-added efficiency, over 8 dB associated gain, and over 10 dB linear gain. The best performance for the Ka-band LNA was over 17 dB gain and 3.5 dB noise figure at Ka-band. In this paper, we report our device, process, and circuit approach to achieve the state-of-the-art performance and producibility of our MMIC chips.**

I. Introduction

GaAs-BASED pseudomorphic HEMT (PHEMT) has emerged as one of the most important technologies for a variety of advanced microwave and millimeter wave systems. It has been used for multifunctional applications such as high power, high efficiency, and low noise at frequencies ranging from C-band up to W-band [1]–[13]. Because of its broad applicability to a multitude of system requirements, there is an ever increasing demand for PHEMT-based products. PHEMT manufacturing technology urgently needs to be developed to cope with this increasing demand at microwave and millimeter wave frequencies.

In the past few years, we have worked intensively on the development of advanced PHEMT technology for microwave and millimeter wave applications. To achieve a high-yield, high-performance PHEMT manufacturing technology, we have optimized both the device epitaxial structure and the fabrication process. We have applied manufacturing disciplines to the PHEMT process and as a result have consistently obtained higher yield, producible and uniform PHEMT's. In addition, with our optimized device epitaxial structure, we have demonstrated superior performance Ka-band multifunctional PHEMT MMIC low noise amplifiers (LNA's), power amplifiers (PA's), mixers, and voltage controlled oscillators (VCO's), all fabricated on the same wafer. The best power performance was demonstrated with a balanced amplifier configuration that yielded an output power of 500 mW with 12 dB associated gain and a power-added efficiency of 32% over the 34–36 GHz frequency range [12]. Low noise amplifiers with a noise figure of 3.5 dB with an associated gain of 17 dB over the 33–37 GHz frequency range have also been demonstrated. Multiple function PHEMT MMIC's on the same wafers have also been successfully fabricated on the ARPA MIMIC Phase 2 program [14].

In this paper, we will present our device epitaxial design, device fabrication process, and MMIC design approach used to achieve these high yield, multifunctional Ka-band PHEMT MMIC's. We also present our wafer lot data in terms of performance, uniformity, and wafer-to-wafer producibility.

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II. Approach

Three key areas were optimized to achieve the results presented in this paper: 1) a PHEMT epitaxial structure that would be process tolerant and yet yield high performance for multiple MIMIC circuit functions; 2) a PHEMT process with broad process margin; and 3) a process tolerant circuit design. We will discuss these in detail in the following sections.

A. PHEMT Epitaxial Design Optimization

Proper PHEMT epitaxial structure design is essential to simultaneously achieve processing margins, particularly for the gate recess process and state of the art device performance. To achieve this we have focused on two critical areas—design and optimization of the GaAs cap layer and the Si planar doping layer. In addition, to obtain the required low phase noise at low frequency for both mixer and oscillator applications, we have utilized low Al content 24%, potentially DX-center-free AlGaAs layers in the device epitaxial structure. We will discuss PHEMT epitaxial design considerations for both mixer and oscillator applications later on this paper.

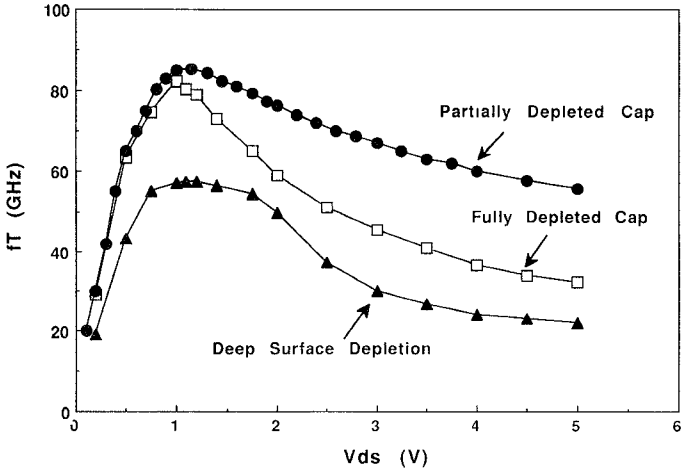


Fig. 1. Cutoff frequency (f_T) as a function of V_{ds} for double-sided doped PHEMT devices having various cap structures. The partially depleted cap structure exhibits relatively flat high f_T values in a broad V_{ds} range, desired for multifunctional applications. Note that the total gatewidth of measured devices is 200–300 μm.

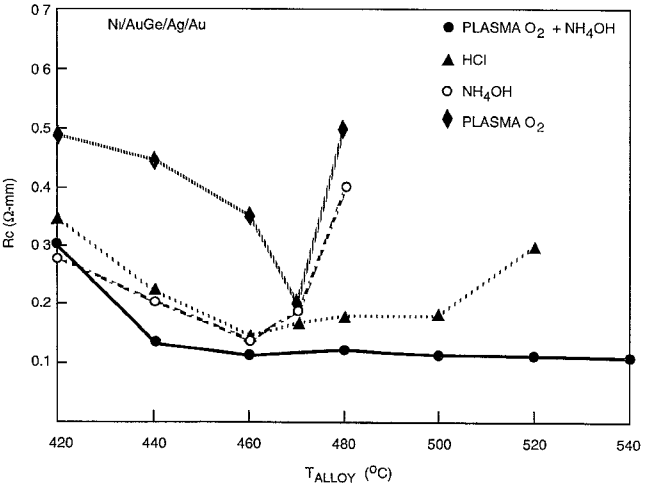


Fig. 2. Contact resistance (R_c) as a function of alloying temperature for Ag barrier ohmic samples using different pre-metal deposition cleaning procedures. The data shows the strong effects of the cleaning procedure on the contact alloying stability and suggests the O_2 plasma + NH_4OH process leads to the cleanest surface and thus a broad optimal temperature range for low R_c.

A. Cap Layer Design

Cap layer design is critical to PHEMT device yield and performance. We have observed that a thin cap layer can lead to high device yield and uniformity. By reducing the thickness of cap layer from 500 Å to 300 Å, both yield and uniformity can be improved by 20–30%. This improvement is the result of a reduction in the variation of gate recess etch depth as the cap layer thickness is decreased. However, the cap layer cannot be too thin (or have too little charge), otherwise it will lead to degradation of device characteristics. A depleted cap layer can lead to a drastic degradation of unity current gain cutoff frequency (f_T), particularly at high drain-source voltage (V_{ds}) ranges. Fig. 1 shows f_T as a function of V_{ds} for various cap structures. f_T remains relatively flat for a partially depleted cap structure, which is desired for all high frequency applications such as power and low noise. On the other hand, the conducting cap (filled with excessive charge) can result in a low breakdown voltage for PHEMT devices because of electric field crowding on the drain side adjacent to the gate fingers. Through judicious selection of the cap layers we have achieved desired saturation current (I_{sat}) values, measured as the current from both cap and channel layers, which also yield high f_t and high breakdown voltage ($8\ V < BV_{ds} < 9\ V$) for millimeter wave applications. This has led to high circuit performance for our multifunctional Ka-band MMIC circuits fabricated on the same wafer.

Si Planar Doping Structure Design: A key focus for our effort was the optimization of the spacer layer thickness and doping concentrations for the Si planar doping layer(s) in the PHEMT structure. The criteria here was to achieve high channel charge density and high carrier mobility. In addition, we evaluated the yield and performance for both single- and double-sided delta-doped structures. We observed that double-sided doped devices exhibit relatively higher noise figure (about 0.1–0.2 dB higher) than single-sided doped devices. This is believed to be due to relatively low carrier mobility often obtained from the double-sided doped structures. In the double-sided doped structure, the reduced carrier mobility can be attributed to the incorporation of Si atoms into InGaAs channel layer from the bottom Si doping layer. In our process, the single-sided delta doped devices exhibited lower yield, poorer uniformity, and lower power characteristics than the double-sided delta-doped devices, despite having lower noise figures. We have attributed the improvement of both device yield and uniformity of the double sided delta doped structure to their relative insensitivity to the variation in the gate recess depth. In terms of power performance, due to their limited channel charge the single-sided doped devices did not generate as much power as the double-sided doped devices.

PHEMT Epitaxial Design Consideration for Mixer and Oscillator Applications: Both mixer and oscillator circuits require high cutoff frequency, high gain, and low noise characteristics. These requirements are the same as for the low noise and power PHEMT amplifiers at Ka-band frequencies. Both of these circuits, however, also require active devices with low phase noise at lower frequencies in order to obtain high spectral purity. AlGaAs layers in the PHEMT structure are used as both a Schottky contact layer and a buffer layer. It is well known that the Si-doped AlGaAs layer is filled with high density of electrically active DX-centers if the Al/Ga ratio is higher than a threshold value of 25%. Note that the DX-centers are electrically deep levels and act as generation-recombination (g-r) centers. They can produce g-r noise and thus low frequency phase noise. The density of these electrically active DX-centers is reduced significantly as the Al content in AlGaAs falls below 25%. Therefore, low Al content in AlGaAs is desired for low phase noise. However, low Al content can lead to poor charge transfer to InGaAs channel layer and thus degrade gain and power characteristics. A 24% Al content in double-sided doped AlGaAs layers and 20% In content in InGaAs channel layer results in channel charge density of $3.2 \pm 0.2 \times 10^{12}\ cm^{-2}$, an excellent compromise for the selected applications here.

An Al content of 24% was selected based on the above considerations. This has resulted in low phase noise performance

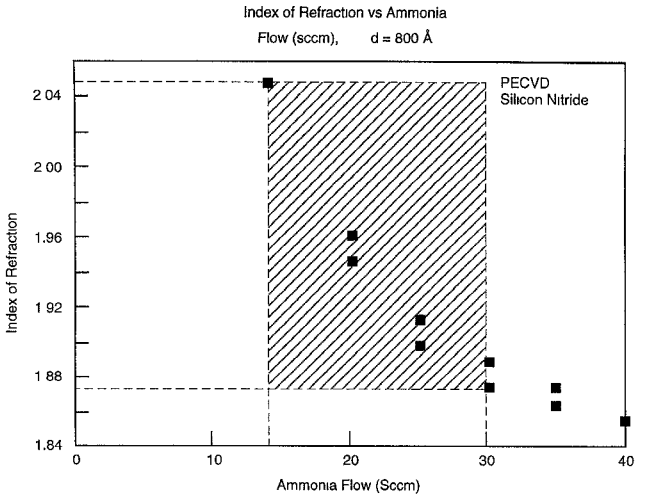


Fig. 3. Index of refraction (n) of the silicon nitride film as a function of ammonia flow rate during the film preparation in the plasma enhanced C_{VD} (PECVD) chamber. We observed that our PHEMT devices exhibited a minimal change in breakdown voltage and other dc characteristics after passivation with PECVD silicon nitride film, deposited at various ammonia flow rate from 14 to 30 sccm. The area within the dotted lines shows the acceptable region of ammonia flow rate and measured refractive index.

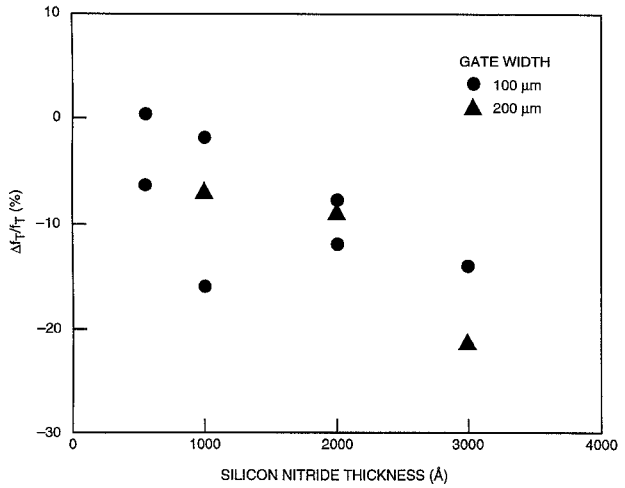


Fig. 4. Reduction in cutoff frequency (f_T) as a function of silicon nitride thickness for PHEMT devices after passivation. A 2000-μm silicon nitride passivation can result in 10–15% reduction in f_T.

for the mixer and oscillator. Note that in contrast to PHEMT, lattice-matched AlGaAs/GaAs HEMT requires high Al content in AlGaAs layers in order to achieve the same level of conduction band discontinuity, channel charge concentration, and charge confinement. As a result of the higher Al content used, AlGaAs/GaAs HEMT's, often exhibits higher phase noise than PHEMT's. Recently, R. Plana *et al.* [15] have reported that PHEMT's exhibit better low frequency noise than FET's and conventional HEMT's. This preliminary result indicates that PHEMT may be suitable for lower frequency low phase noise applications, in addition to the millimeter wave low noise and power applications.

B. Manufacturable PHEMT Process Development

Broad process margin is key to a high yield manufacturing process. In the PHEMT process development, we have

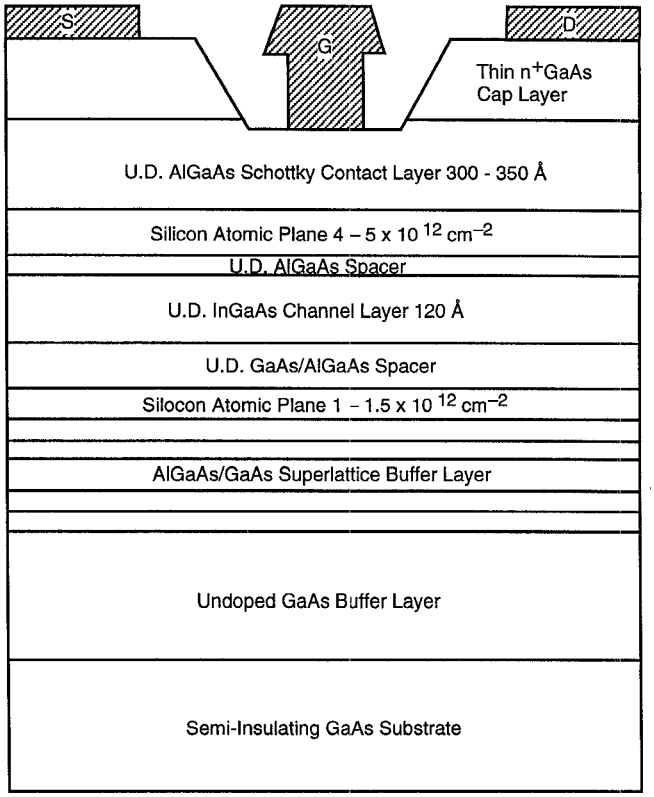


Fig. 5. Our baseline, thin cap, double-sided doped PHEMT structure. The cap layer of the structure is partially depleted. Using a single-gate recess process, devices fabricated on this structure have demonstrated multifunctional Ka-band MMIC performance.

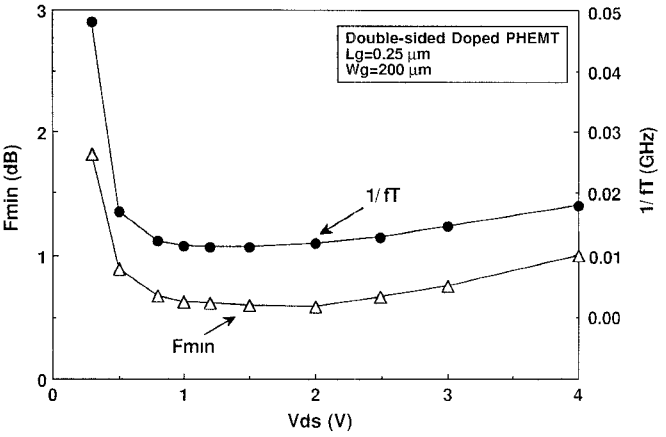
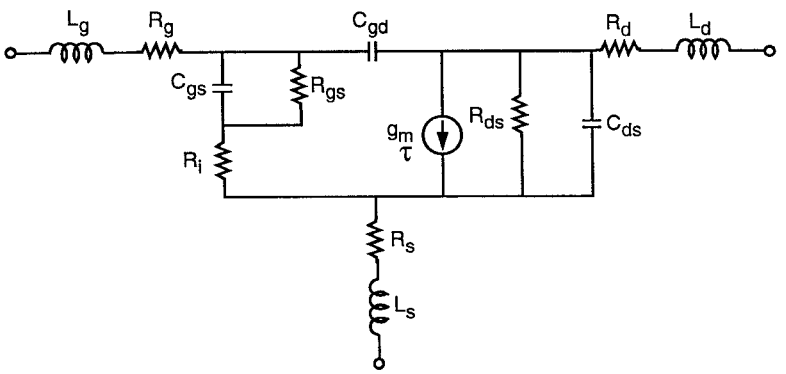


Fig. 6. Minimum noise figure $(F_{\min})$ at 10 GHz and $1/f_T$ as a function of V_{ds} for our baseline PHEMT devices. $F_{\min}$ values are low (0.6–1.0 dB) in a broad V_{ds} range (0.5–4 V). $F_{\min}$ shows a close correlation with $1/f_T$.

optimized several critical process steps. We present two key studies and their results in the following sections.

Ohmic Contact Process: We extensively studied the Ag barrier ohmic metal contacts for PHEMT. Our results indicate a strong dependence of ohmic contact characteristics on the pre-metal-deposition cleaning procedure. As shown in Fig. 2, the ohmic sample pre-cleaned with combined a O_2 plasma and NH_4OH process exhibited a very broad optimal alloy temperature window (440°C–540°C), outperforming other samples cleaned by other techniques [16]. This suggests a noncritical alloy process for our optimized ohmic contact process.



$W_g = 4 \times 50\ \mu m$, $V_{ds} = 3V$. $V_{gs} = -0.99$ V, $I_{ds} = 25$ mA

g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	τ (ps)	R_g (Ω)	R_{gs} (KΩ)	R_i (Ω)	R_s (Ω)	R_{ds} (Ω)	R_d (Ω)	L_g (pH)	L_s (pH)	L_d (pH)	f_T (GHz)
110.0	231.6	46.0	73.2	0.41	1.29	3.41	1.85	1.8	158.0	8.59	34.8	1.3	25.0	64.8

Fig. 7. Equivalent circuit element values for our devices ($Lg = 0.25\ \mu$m, $Wg = 4 \times 50\ \mu$m).

Silicon Nitride Passivation: We found that the PHEMT devices exhibited a minimal change in breakdown voltage and other dc characteristics after passivation with plasma enhanced chemical vapor deposited (PECVD) silicon nitride film, deposited at various ammonia flow rates from 14 to 30 sccm. Fig. 3 shows the relation between ammonia flow rate and measured refractive index of the deposited silicon nitride. The area within the dotted lines show an acceptable region of ammonia flow rate and measured refractive index, where the PHEMT devices exhibited less than 0.5 V change in breakdown voltage after passivation. This suggests a broad deposition process margin for our silicon nitride as a passivation layer for PHEMT devices.

However, as other researchers have reported, we observed a degradation of f_T by 10–15% for the PHEMT devices for silicon nitride passivation thicknesses beyond 2000 Å, as shown in Fig. 4. The exact causes of this degradation are complex and are still under investigation. But it is certain that part of the degradation is due to the increase in gate capacitance in response to the presence of high dielectric constant silicon nitride surrounding the gate finger region. Nevertheless, we have controlled the run-to-run variation of f_T after passivation within $\pm 7\%$ for the 0.25-μm PHEMT devices.

III. Device and MMIC Fabrication

The device epitaxial structure utilized in this work is a double-sided delta-doped AlGaAs-InGaAs-GaAs PHEMT shown in Fig. 5. The structure was grown by MBE on a semi-insulating GaAs substrate. Typical values obtained from Hall measurement for the InGaAs channel sheet charge density and room temperature carrier mobility are $3.2 \pm 0.2 \times 10^{12}$ cm^{-2} and 5300–5600 cm^2/V-sec, respectively. The gate contact AlGaAs layer was undoped so that a suitably high gate-drain breakdown voltage can be achieved.

We etched a mesa structure for device isolation and utilized low contact resistance AuGe-based alloyed ohmic contacts for both the source and drain. We employed low-resistance mushroom gates. The gates were defined in PMMA/PMAA bilayer resist by e-beam lithography using a Philips Beamwriter machine. The gate length is 0.25 μm. After gate recess etching, a Ti-Pt-Au metal system was evaporated onto the gate opening region and lifted off to form gate fingers.

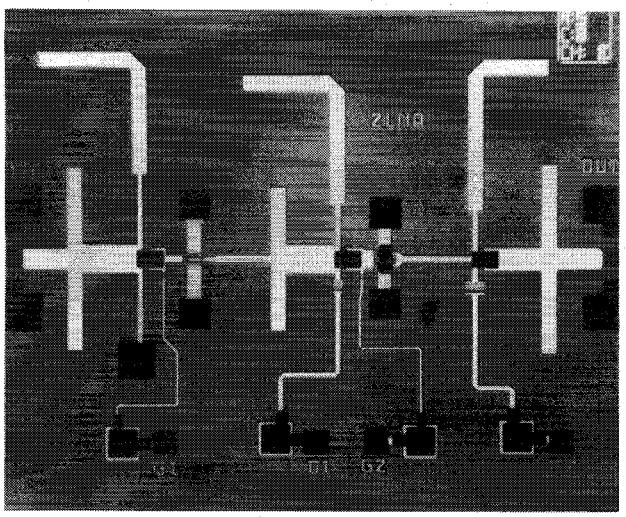
Other MMIC components fabricated include TaN resistors, Ti-Au transmission lines, dielectric capacitors, and Au-plated airbridges. After completing front-side processing, thinned the substrate to 4 mils, etched via holes and metallized the backside with Au. The device results reported here come from several different PHEMT wafers. The MMIC results presented in this paper were measured on two device lots, each containing four PHEMT wafers with the above structure.

IV. Device Peripheries

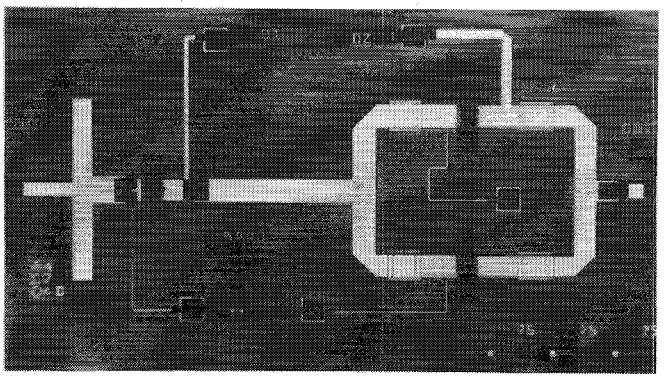
To simplify device characterization, we employ devices with only 50- and 75-μm unit gate fingers. For example, a 100-μm FET in the low noise amplifier consists of two gate fingers each with a 50 μm width, while a 450-μm FET in the power amplifier employs six 75-μm unit gate fingers. This arrangement allows for easier device scaling and FET model verification. Typical dc bias conditions for these FETs are 25% I_{dss} and 50% I_{dss} for low noise and power operation, respectively.

V. Device Results

The fabricated PHEMT's typically exhibited a full-channel drain current density (I_{max}) of over 600 mA/mm and a peak transconductance (g_m) of 400–450 mS/mm. The source-drain breakdown voltage (BV_{ds}) was 8–9 V and pinch off voltage (V_{po}) was -1.1 V. The power device ($< 400\ \mu$m) typically exhibited output power density of 700–800 mW/mm with



(a)



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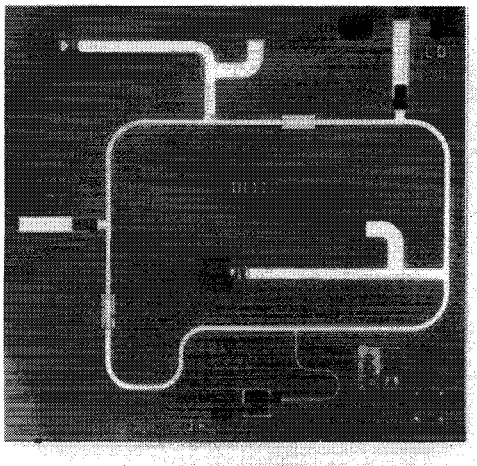
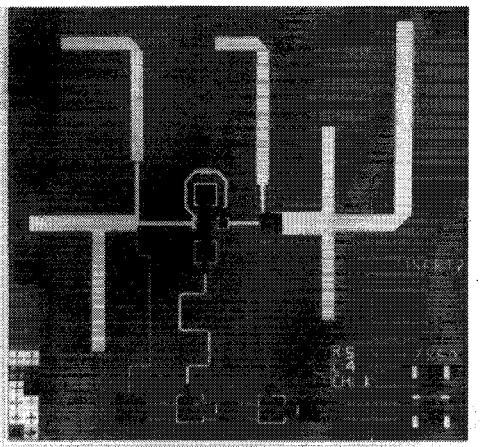
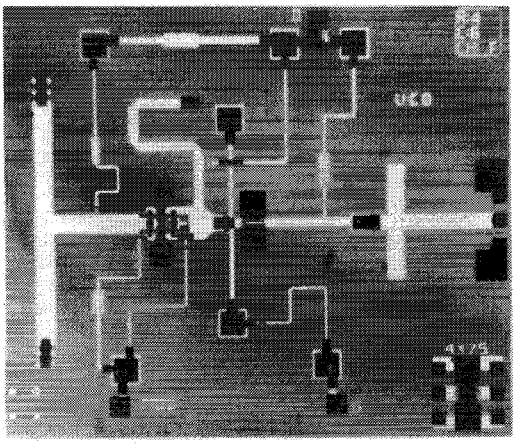
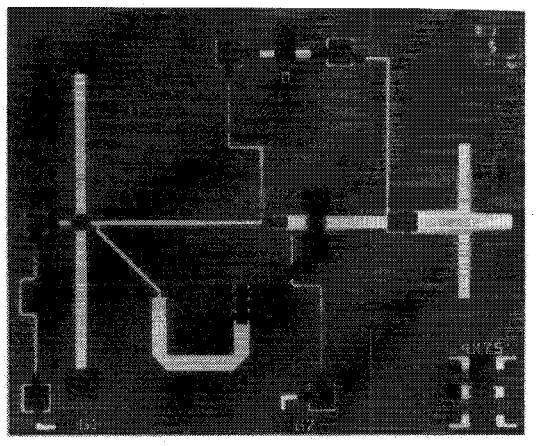




DIODE RING MIXER FET MIXER

(c)





RING VCO SHORTED GATE VCO

(d)

Fig. 8. (a) Two-stage PHEMT Ka-band MMIC low noise amplifier. Chip size is 1.875 × 2.25 mm. (b) PHEMT Ka-band MMIC balanced power amplifier. Chip size is 1.875 × 3.25 mm. (c) PHEMT Ka-band diode ring and FET mixers. Individual chip size is 1.875 × 2.00 mm. (d) PHEMT Ka-band ring and shorted-gate voltage controlled oscillators (V_{CO}). Individual chip size is 1.875 × 2.25 mm.

power-added efficiency of 35–40%. A typical 100-μm device biased at 25%I_{dss} exhibited a noise figure of approximately 0.6 dB at 10 GHz and 1.2 dB at 18 GHz. Fig. 6 shows the device F_{min} versus V_{ds}. Because of the relative insensitivity

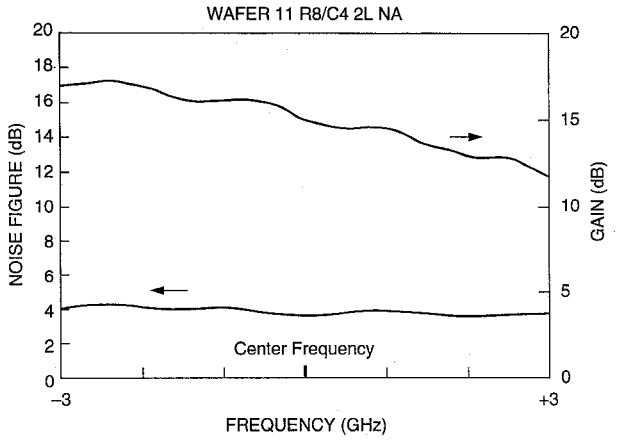


Fig. 9. The performance of both noise figure and gain in Ka-band range for our 2-stage LNA. The LNA exhibits a noise figure between 3.5 and 5.0 dB, across the 5-GHz bandwidth.

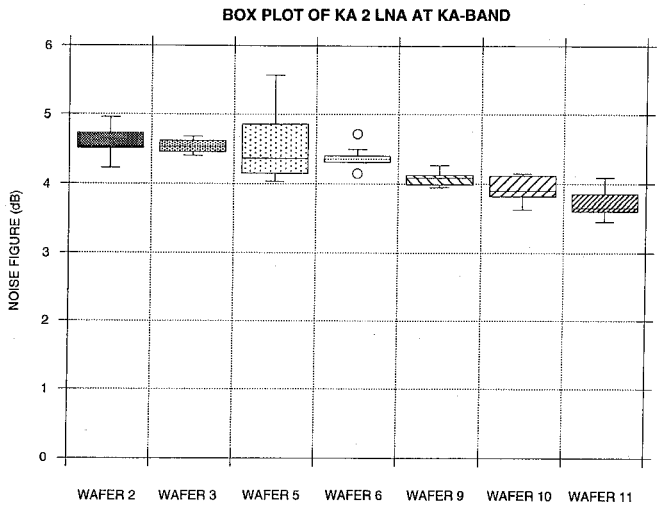


Fig. 10. Noise performance of LNA's from seven wafers tested. The noise performance distribution was uniform from wafer to wafer. The improvement of noise performance for the later three wafers is due to circuit redesign.

of f_T to variations in $V_{\rm ds}$ and low gate leakage, the optimized double-sided doped structure showed a broad low $F_{\rm min}$ range. In addition, the devices exhibited a relatively broad low $F_{\rm min}$ range as a function of $I_{\rm ds}$ as a result of slowly varying g_m and f_T. Both are desired characteristics for low noise amplifier designs.

We have consistently achieved high yield, high producibility, and high uniformity device results using the above manufacturable processes and designs. We have recently repeated our results on the PHEMT wafer lots fabricated for the MIMIC Phase 2 program. The wafers exhibited uniform values of both $I_{\rm dss}$(at $V_g = 0$ V) and $V_{\rm po}$ with only 13% deviation across the 3-in. wafers. Wafer-to-wafer uniformity is excellent: $I_{\rm dss}$ is 360 $\pm$ 1.7 mA/mm, and $V_{\rm po}$ is -1.09 ± 0.04 V for a 4-wafer lot. In addition, the f_T values are tightly grouped at 61.32 $\pm$ 2.45 GHz across a 3-in. wafer measured at $V_{\rm ds}$ of 3 V. Fig. 7 shows typical extracted circuit element values for our devices.

VI. MMIC Circuit Technology

Four major Ka-band MMIC transceiver components were designed and fabricated to demonstrate the feasibility of our

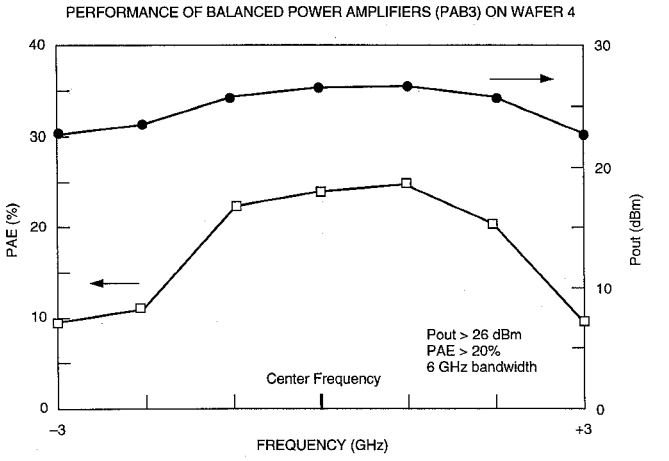


Fig. 11. Typical output power characteristics of our Ka-band balanced power amplifiers.

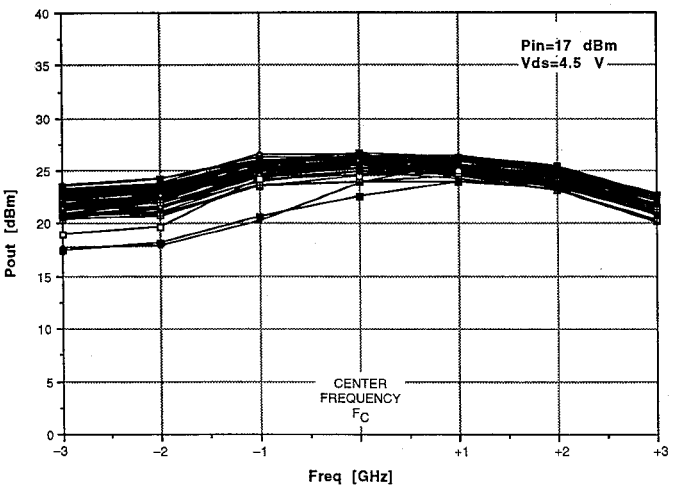


Fig. 12. Ka-band power amplifier power performance on a 3-in. PHEMT wafer. The power output of 49 MMIC's is shown on this wafer.

PHEMT manufacturing technology. As mentioned previously, the circuits are low noise amplifiers, power amplifiers, mixers, and voltage-controlled oscillators. The circuits were designed to achieve high performance with these goals in mind: high yield, good uniformity, and producibility. A rapidly maturing fabrication technology and advances in microwave CAD tools have allowed circuit design at Ka-band to be much more straightforward. Designing a millimeter-wave circuit that is insensitive to process variation, however, is still an area that needs considerable work. A 14-element equivalent circuit model is typically employed in circuit design. A device model with physical representation can often be used to compare process variations from lot to lot. The proper matching circuit topology is important since it can minimize circuit performance variation. Fig. 8(a)–(d) shows photographs of the Ka-band circuits fabricated on 3-in. PHEMT wafers.

A. Low-Noise Amplifier

The two-stage low noise amplifier consists of two single-ended stages cascaded in series. A 100-μm device was employed in the first stage to drive a 200-μm device in the second stage. The input matching circuit of the LNA was designed for optimum noise performance, while maintaining a good input

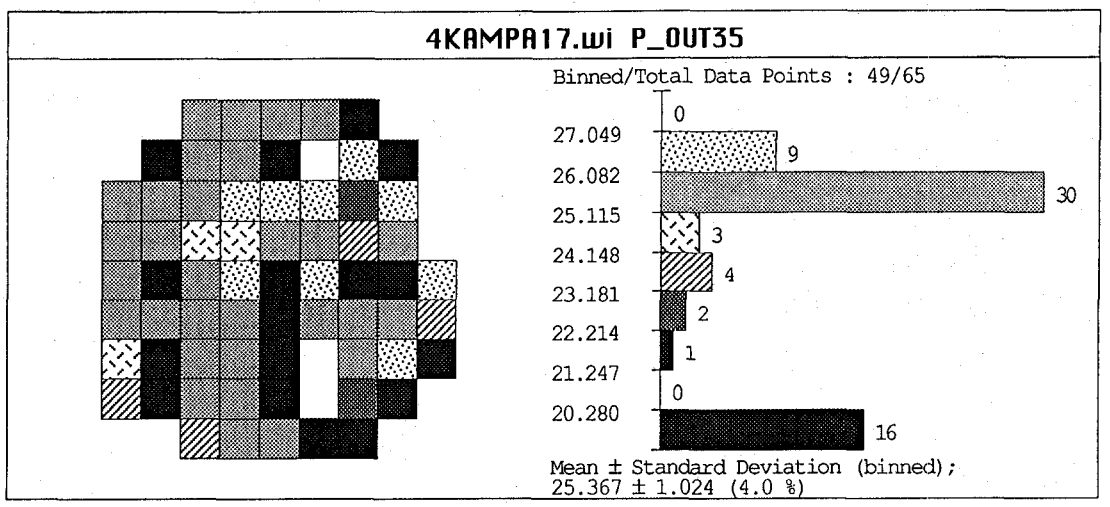


Fig. 13. RF power output wafer map of a Ka-band PHEMT wafer. Average output power is 25.4 dB with 4% uniformity over the wafer.

return loss. The second stage amplifier was designed to provide high gain. On-wafer S-parameters measured up to 40 GHz and noise parameters characterized up to 18 GHz were utilized in the design.

B. Power Amplifier

The power amplifier employs a 300-μm device in the first stage to drive a set of two 450-μm FET's in the output stage. The circuit consists of mainly microstrip transmission lines which have the advantage of 1) reduced uncertainty in passive element circuit models and 2) reduced coupling between circuit elements. The input matching circuit consists of open circuit stubs and the output matching circuit consists of microstrip transmission lines that serve as an impedance transformer. Both interstage and output matching circuits were designed using a load line technique. The dc bias line was designed using quarter-wavelength transmission lines that present an open circuit to the matching network at the designed frequency, eliminating loading effects.

C. Mixers

Two types of mixers were designed: FET mixer and diode mixer.

FET Mixer: A FET mixer was designed utilizing the time varying channel resistance of a HEMT device in the linear region. A LO signal, pumping at the gate port, modulates the channel resistance to create frequency mixing with a RF signal coupled to the drain. An IF output is obtained at the source. The conversion loss of the FET mixer is determined by the on and off ratio of the channel resistance, therefore the performance is less sensitive to process variations. Input matching circuit was designed based on the small signal equivalent circuit model, and the output-matching circuit was designed using the effective channel resistance under LO drive. A transmission line is connected between the drain and gate ports to provide parallel resonance with the drain to gate capacitance $C_{\rm dg}$. This minimizes the LO signal coupling to the drain port, greatly improving the gate to drain isolation. The IF frequency is so low that the matching circuit is not critical.

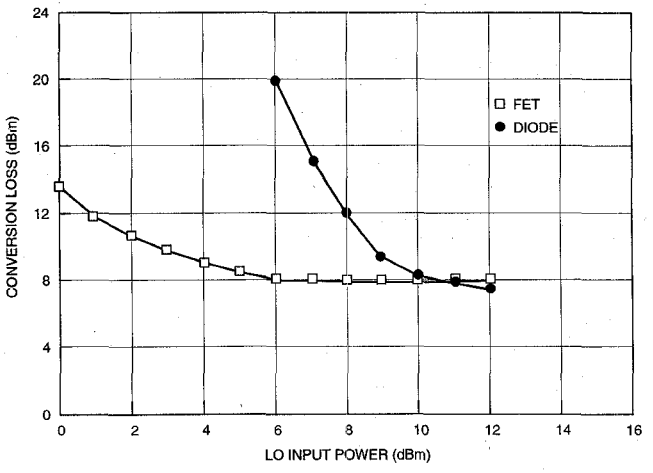


Fig. 14. Comparison of conversion loss for both FET and diode mixers at various LO powers.

Diode Mixer: A 180-degree rat-race circuit is employed in the diode mixer to drive a pair of diodes 180 degrees out of phase. It then recombines maximally in phase at the IF frequency. Since the mixer operates on the diode's on and off states, the conversion loss is more sensitive to process variations. It also requires a high LO signal to drive the mixer.

D. Voltage-Controlled Oscillators (VCO's)

Two types of VCO circuits were designed: a ring VCO and a shorted gate VCO.

Ring VCO: The ring VCO was designed by utilizing an active device as a feedback element to form a ring-type oscillator. The matching circuit was designed to maximize the negative resistance at the drain. A buffer amplifier at the oscillator output port, was employed to boost the output power and minimize frequency pulling due to external loading.

Shorted Gate VCO: A 100-μm PHEMT device was used in a common source configuration to realize a shorted gate oscillator. This design was used to obtain better phase noise at the expense of reducing the tuning bandwidth. As with the ring VCO, the shorted gate VCO utilized a buffer amplifier to boost the output power and minimize frequency pulling.

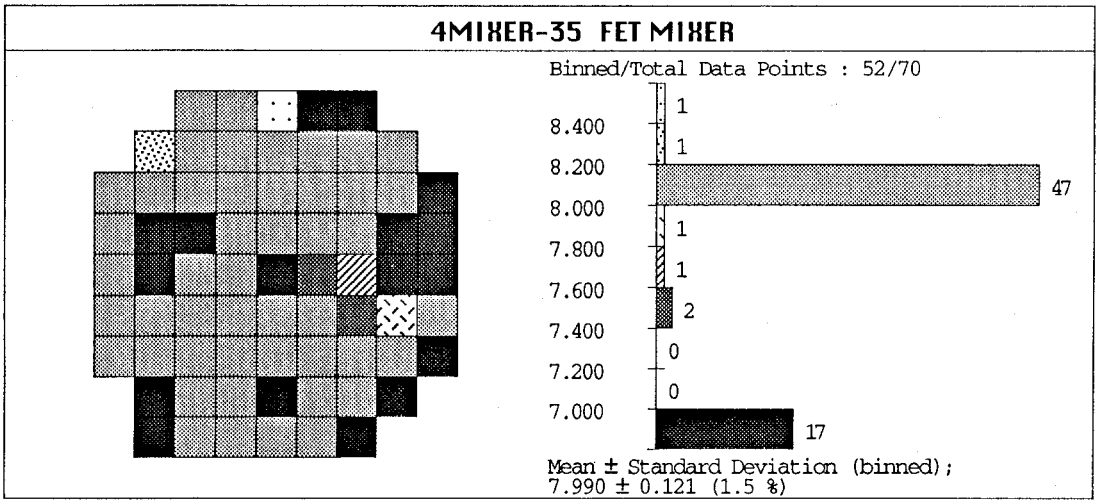


Fig. 15. Wafer map of conversion loss of FET mixers.

VII. MMIC Measurements and RF Results

We performed 100% on-wafer measurements for the power amplifiers, diode mixers, FET mixers, LNA's and the oscillator circuits. It should be noted that all measurements were carried out at a constant bias, i.e. the circuits were biased at a constant voltage and current, as opposed to individual bias tuning for each circuit, as reported in some previous publications.

The two-stage LNA exhibited a noise figure between 3.5 and 5.0 dB, across the 5-GHz bandwidth around center frequency at Ka-band. The gain performance of the LNA is as high as 17 dB at 33 GHz, as shown in Fig. 9. The noise performance distribution was uniform from wafer to wafer (the noise performance of seven wafers is shown in Fig. 10, measured at nine test sites on each wafer). The LNA circuit was redesigned and improved for wafers 6–11, and this resulted in lower noise figures (as low as 3.5 dB on wafer 11).

The power amplifiers were measured under both small and large signal conditions. Excellent performance was obtained at Ka-band: an output power of over 26 dBm and a power-added efficiency exceeding 20% were achieved with an associated gain of over 9 dB. Fig. 11 shows output power characteristics of a typical PHEMT wafer, measured across a 6-GHz bandwidth in Ka-band, with 17-dBm input power. A composite plot of 49 2-stage power amplifiers is shown in Fig. 12, exhibiting a tight distribution. Fig. 13 shows output power uniformity for the power amplifiers, with an average output power of 25.37 dBm and a standard deviation of 4% measured at 35 GHz. The tight distribution is shown in the histogram shown on the right side of the figure. There are 9 test reticles and 2 dropouts among the 21 data points that are excluded from the mean output power calculation.

Both FET and diode mixers were measured with 10 dBm LO input power and -5 dBm RF input power at the center of the frequency band. Fig. 14 shows the conversion loss of a typical FET mixer compared with a diode mixer at various LO powers. Both mixers achieved a conversion loss of 7.8 dB at around 10 dBm LO drive. However, a FET mixer requires a much lower LO power to operate. A wafer map of FET mixer conversion loss is shown in Fig. 15. Excellent uniformity was obtained with an average conversion loss of 8.0 dB and a standard deviation of 2%. The average diode mixer conversion loss is 8 dB with a standard deviation of 4%. The FET mixer exhibits superior uniformity as compared with diode mixers due to the mixing mechanism as described in the previous section. The best wafer exhibited an average conversion loss of 6.55 dB for FET mixers and 7.14 dB for diode mixers.

We also tested two types of VCO's fabricated on the same PHEMT wafers. On one wafer, the average output power was 15.8 ± 1.0 dBm for the ring VCO and 11.5 ± 1.5 dBm for the shorted gate VCO. The phase noise is about -85 dBc/Hz for ring VCO and -90 dBc/Hz at 1 MHz away from the center frequency.

The above results demonstrate that we have obtained state-of-the-art multifunctional performance from these PHEMT wafers, using four types of circuits fabricated on the same wafer.

VIII. Conclusion

We have demonstrated the feasibility of PHEMT manufacturing technology. Multiple circuit performance was measured across the entire wafer under fixed bias conditions, with no attempt to optimize performance of each chip by adjusting its dc bias individually, as opposed to others reporting one of a type of performance based on individual circuit optimization.

To the best of our knowledge, this is the first paper to report truly multifunctional PHEMT circuits with uniform RF performance on the same wafer at millimeter wave frequencies.

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W. Yau, photograph and biography unavailable at time of publication.

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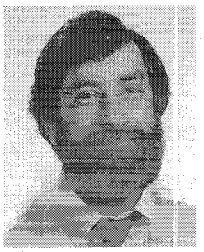
S. X. Bar, photograph and biography unavailable at time of publication.

A. Kurdoghlian, photograph and biography unavailable at time of publication.



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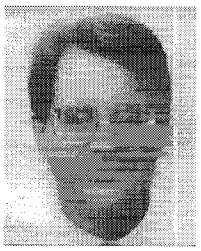

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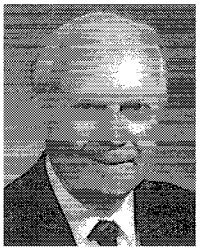

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